REMARKS

Present Status of the Application

The Office Action rejected claims 1 and 13, objected claims 2-7 and 14-20, and allowed claims 8-12. Specifically, the Office Action rejected claims 1 and 13 under 35 U.S.C. 103(a), as being unpatentable over Wu et al. (US No. 6,263,397) in view of Chen et al. (US No. 6,301,630). The Office Action objected claims 2-7 and 14-20 as being dependent upon a rejected base claim. Further, the Office Action allowed claims 8-12. Applicants have deleted claims 1 and 13, amended claims 2 and 14 to improve clarity, and added new claims 21-27. After entry of the foregoing amendments, claims 2-12 and 14-27 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of objections

According to the Office Action, claims 2-7 and 14-20 are objected to as being dependent upon a rejected base claim. To overcome this issue, Applicants have amended claims 2 and 14 to be patentable independent claims, and therefore claims 2-7 and 14-20 are patentable.

Discussion of Office Action Rejections

The newly added claims 21-27 are patentable over Wu in view of Chen.

Firstly, Wu and Chen cannot be combined together. More specifically, according to Wu's specification and drawings, I/O agent writes interrupt message to chipset to *initiate* interrupt

transaction (Step 220 in FIG.4). Therefore, *Wu monitors the write transaction (hereinafter, first write transaction) which writes the interrupt message to chipset*. Furthermore, before monitoring the first write transaction, Wu flushes the buffer queue in the chipset to the main memory in Step 215. However, a write transaction (hereinafter, second write transaction) determines an associated buffer set in Chen, and the determined associated buffer set is flushed thereafter. Accordingly, *the first write transaction is generated after the buffer is flushed, but the second write transaction is generated before the buffer is flushed*. That is, **the two write transaction in Wu and Chen respectively is generated at different bus timing and those skilled in the art cannot combine the two citations together.**

In other words, Wu uses a first write transaction to start an interrupt sequence, and Chen determines a buffer set by monitoring a second write transaction. Because the first write transaction is generated after the buffer set is flushed while the second write transaction is the content of the flushed buffer set, combination of Wu and Chen may conflict on bus timing and therefore the combination should not be achieved.

Secondly, if the Examiner insists that Wu and Chen could be combined together, it is very obvious that combination of Wu and Chen did not disclose, teach or suggest the feature of "monitoring a memory write transaction whose address falls into a reserved interrupt address located in the system memory; and performing an interrupt sequence when the monitored memory write transaction is sent on the PCI bus." as claimed in claim 21. More specifically, as discussed above, the first write transaction is different from the second write transaction. *Although the second write transaction might specify a predetermined buffer set*, the second write

transaction cannot be used to determining whether the interrupt sequence should be performed or not *since Wu determines that according to the first write transaction, which is generated after the buffer set is flushed.* In another respect, although Wu monitors the first write transaction, it cannot determine which buffer set is to be used.

In other words, by combining Wu and Chen, those with ordinary skill might determine a buffer set by monitoring the second write transaction before the buffer set is flushed, and after the buffer set is flushed, a first write transaction might start an interrupt sequence. However, **those with ordinary skill uses two write transaction to complete the operation, while the present invention uses only one memory write transaction**.

Accordingly, claim 21 is patentable over Wu in view of Chen because combination of Wu and Chen did not disclose, teach or suggest the feature as claimed in claim 21, or, in another respect, Wu and Chen cannot be combined together.

Claims 22-27 are patentable over Wu in view of Chen as a matter of law since claim 21, on which claims 22-27 depends, is patentable.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 2, 8, 14 and 21 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3-7, 9-12, 15-20 and 22-27 patently define over the prior art as well.

Application No.: 09/826,784 **Docket No.: JCLA6095**

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 2-12 and 14-27 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

Date: 9/7/2004

Jiawei Huang
Registration No. 43,330

4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761
Fax: (949) 660-0809